AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording, using the same recorder, said apparatus comprising:

a frequency conversion circuit for converting an inputted 32T-cycle binarized wobble signal based on a DVD+RW/+R standard into a 186T-cycle binarized wobble signal based on a DVD-R/RW standard;

a selector for selecting, as a selected 186T-cycle binarized wobble signal, either the converted 186T-cycle binarized wobble signal that is outputted from the frequency conversion circuit ~~or the inputted~~ or an inputted 186T-cycle binarized wobble signal, and outputting the selected 186T-cycle binarized wobble signal; and

a PLL circuit for 186-multiplying the frequency of the selected 186T-cycle binarized wobble signal ~~on receipt of the output of~~ outputted from the selector.

2. (Currently Amended) A recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording, using the same recorder, said apparatus comprising:

a frequency conversion circuit for converting an inputted 186T-cycle binarized wobble signal based on a DVD-R/RW standard into a 32T-cycle binarized wobble signal based on a DVD+RW/+R standard;

a selector for selecting, as a selected 32T-cycle binarized wobble signal, either the converted 32T-cycle binarized wobble signal that is outputted from the frequency conversion circuit ~~or the inputted~~ or an inputted 32T-cycle binarized wobble signal, and outputting the selected 32T-cycle binarized wobble signal; and

a PLL circuit for 32-multiplying the frequency of the selected 32T-cycle binarized wobble signal ~~on receipt of the output of~~ outputted from the selector.

3. (Currently Amended) A recording clock generation apparatus as defined in Claim 1 further

including a physical address data decoder comprising a circuit for converting a binarized ADIP signal based on the DVD+RW/+R standard into a binarized land pre-pit signal based on the DVD-R/RW standard, and a circuit for detecting even sync data, odd sync data, 0 data, and 1 data from the binarized land pre-pit signal.

4. (Currently Amended) A recording clock generation apparatus as defined in Claim 2 further including a physical address data decoder comprising a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on the DVD+RW/+R standard, and a circuit for detecting sync data, 0 data, and 1 data from the binarized ADIP signal.

5. (Currently Amended) A recording clock generation apparatus as defined in Claim 1 further including:

a circuit for converting a binarized ADIP signal based on the DVD+RW/+R standard into a binarized land pre-pit signal based on the DVD-R/RW standard; and

a phase adjustment circuit for performing phase adjustment between the selected 186T-cycle binarized wobble signal and the binarized land pre-pit signal which are based on the DVD-R/RW standard.

6. (Currently Amended) A recording clock generation apparatus as defined in Claim 2 further including:

a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on the DVD+RW/+R standard; and

a phase adjustment circuit for performing phase adjustment between the selected 32T-cycle binarized wobble signal and the binarized ADIP signal which are based on the DVD+RW/+R standard.

7. (Currently Amended) A recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording, using the same recorder, said apparatus comprising:

a frequency conversion circuit for converting an inputted first cycle binarized wobble signal based on a first optical disc standard into a second cycle binarized wobble signal based on a second optical disc standard;

a selector for selecting, as a selected second cycle binarized wobble signal, either the second cycle binarized wobble signal that is outputted from the frequency conversion circuit or ~~the inputted first~~ an inputted second cycle binarized wobble signal, and outputting the selected second cycle binarized wobble signal; and

a PLL circuit for multiplying the frequency of the selected second cycle binarized wobble signal outputted from the selector to change its cycle from the wobble cycle to the cycle of the recording clock~~, on receipt of the output of the selector~~.